WHAT IS CLAIMED IS:

1. A method for reducing power consumption in a memory circuit, comprising, a pre-charged stage coupled to an evaluation stage by at least an internal node, said method comprising:

setting an input of said pre-charged stage to a first high logic level;

responsive to said setting said input, setting said internal node to a first low logic level within a first transparency window;

responsive to said setting said internal node, said evaluation stage changing said output of said evaluation stage to a second high logic level within said first transparency window; and

when said input remains at said first high-logic level, maintaining said internal node at said first low logic level through at least a second transparency window.

2. The method of claim 1 wherein said transparency window comprises when said internal node is logically equivalent to an inverted input.

3. The method of claim 1 wherein said second transparency window is a transparency window subsequent to said first transparency window.

4. The method of claim 1 wherein said memory circuit is a flip-flop.

5. The method of claim 4 wherein said flip-flop is a D type flip-flop.

6. The method of claim 1 wherein said maintaining said internal node at said first low logic level includes maintaining said output at said second high logic level.

7. The method of claim 1 further comprising, after said first transparency window, if said input transitions from said first high logic level to a second low logic level, setting said internal node to a third high logic level until at least said second transparency window.

8. A conditional pre-charged system for reducing power consumption in a memory circuit comprising:

a pre-charge stage for determining a pre-charge stage output depending upon a data input and a data output during a transparency window; and

an evaluation stage for evaluating said pre-charge stage output to produce said data output during said transparency window;

wherein when said data input and said data output have high logic levels, said pre-charge stage output has a low logic level; and

wherein when said data input and said data output have said high logic levels through a subsequent transparency window, said pre-charge stage output remains at said low logic level through said subsequent transparency window.

9. The conditional pre-charged system of claim 8 further comprising a first clock for activating said pre-charged stage, and a second clock for activating said evaluation stage, wherein said second clock comprises said first clock inverted and delayed.

10. The conditional pre-charged system of claim 8 wherein said first transparency period comprises when said first clock and said second clock both have high logic levels.

11. The conditional pre-charged system of claim 8 wherein said evaluation stage comprises a conditional keeper.

12. The conditional pre-charged system of claim 11 wherein said conditional keeper comprises an inverter coupled to a tri-state inverter.

13. The conditional pre-charged system of claim 8 wherein said evaluation stage comprises an unconditional keeper.

14. The conditional pre-charged system of claim 13 wherein said unconditional keeper comprises back-to-back inverters.

15. The conditional pre-charged system of claim 8 wherein said data output is feedback into said pre-charge stage.

16. The conditional pre-charged system of claim 8 wherein said pre-charge stage comprises a conditional keeper.

17. The conditional pre-charged system of claim 8 wherein said pre-charge stage comprises an unconditional keeper.

18. The conditional pre-charged system of claim 17 wherein said unconditional keeper comprises an nMOS and a pMOS transistor.

19. The conditional pre-charged system of claim 8 wherein said memory circuit is a flip-flop.

20. A conditional pre-charged system for reducing power consumption in a memory circuit comprising:

a pre-charge stage for determining a pre-charge stage output depending upon a data input during a transparency window, wherein said pre-charge stage output is feedback into said pre-charge stage;

an evaluation stage for evaluating said pre-charge stage output to produce a data output during said transparency window;

wherein when said data input and said data output have high logic levels, said pre-charge stage output has a first low logic level; and

wherein when said data input transitions to a second low logic level before a subsequent transparency window, said pre-charge stage output is set to a high logic level at least until said subsequent transparency window.

21. The conditional pre-charged system of claim 20 wherein said evaluation stage comprises a conditional keeper.

22. The conditional pre-charged system of claim 20 wherein said conditional keeper comprises an inverter coupled to a tri-state inverter.

23. The conditional pre-charged system of claim 20 wherein said evaluation stage comprises a conventional keeper.

24. The conditional pre-charged system of claim 23 wherein said unconditional keeper comprises back-to-back inverters.

25. The conditional pre-charged system of claim 20 wherein said pre-charge stage comprises a conditional keeper.

26. The conditional pre-charged system of claim 20 wherein said pre-charge stage comprises an unconditional keeper.

27. The conditional pre-charged system of claim 26 wherein said unconditional keeper comprises an nMOS and a pMOS transistor.

28. The conditional pre-charged system of claim 20 wherein said memory circuit is a flip-flop.

29. A conditional pre-charged system for reducing power consumption in a flip-flop comprising:

a first means for determining a pre-charge output depending upon a data input and a data output during a transparency window;

a second means for evaluating said pre-charge output to produce said data output during said transparency window; and

a keeper means for maintaining said data output between transparency windows;

wherein when said data input and said data output have high logic levels, said pre-charge output has a low logic level ; and

wherein when said data input and said data output have said high logic levels through a subsequent transparency window, said pre-charge output remains at said low logic level through said subsequent transparency window.